This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-8. (cancelled)

9. (original) In a process for forming an interconnect including the steps of patterning a photoresist mask featuring masked areas corresponding to a critical dimension, and then etching an underlying interconnect metallization layer in unmasked areas to leave adjacent first and second metal lines having a width corresponding to the critical dimension, a method for reducing variation in parasitic capacitance between the metal lines attributable to a variation in critical dimension, the method comprising the steps of:

determining a range of critical dimensions exhibited by a photolithography process; and

simulating variation in parasitic capacitance over the critical dimension range by determining the extent of penetration of an overlying third metal line into an inter-line region between the metal lines, a width of the inter-line region determined by a thickness of the conformal middle interlayer dielectric and by the critical dimension, such that penetration of the third metal line elevates parasitic capacitance while reducing parasitic capacitance variation over the critical dimension range.

10. (original) In a process for forming an interconnect including the steps of patterning a photoresist mask featuring masked areas corresponding to a critical dimension, etching an underlying interlayer dielectric in unmasked areas to leave adjacent first and second trenches having a width corresponding to the critical dimension, and then filling the first and second trenches with interconnect metallization to form first and second metal lines, a method for reducing variation in parasitic capacitance between the metal lines attributable to a variation in critical dimension, the method comprising the steps of:

determining a range of critical dimensions exhibited by a photolithography process; and

simulating variation in parasitic capacitance over the critical dimension range by determining the extent of penetration of an overlying third metal line into an inter-line region between the metal lines, a width of the inter-line region determined by a thickness of the conformal middle interlayer dielectric and by the critical dimension, such that penetration of the

third metal line elevates parasitic capacitance while reducing parasitic capacitance variation over the critical dimension range.

Claims 11-15. (Cancelled.)